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Synthesis and fabrication of gold nanoparticles thin films and their applications in non-volatile organic memory devices

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Outline

Introduction

The market for non-volatile memory (NVM) devices is growing rapidly because of their high demand in portable electronics, such as mobile phones, digital cameras, and hard drives [1-3]. A NVM with a three-terminal structure comprises a source, a drain, a control dielectric gate, and a floating gate (FG) [4]. NVM retains stored data when electrical power is turned off. NVM devices, such as flash memory based on FG, feature a massive memory capacity. However, the application of this flash memory device is limited by continuous scaling down of device size. Scaling down device size induces significant leakage current and causes power consumption during reading and programming. An alternative path is to replace the FG with a discrete charge-trapping material. Discrete charge-trapping layers with nanoparticle memory devices embedded in the dielectric layer have been studied actively by researchers to address the dilemma in device scaling down [2]. A high-performance organic memory with discrete nanoparticles embedded in the organic dielectric layer will contribute to the rapid development of information technology, including personal computers, mobile phones, digital cameras, and media players, which have become an essential part of our daily life and an important player in transparent electronics [5].

Information is stored in the trapping layer of discrete nanoparticles embedded in dielectric layer memory. Memory devices containing semiconductor nanoparticles such as Si and Ge have drawn considerable attention as replacement to conventional FG flash memory devices [6, 7]. A flash memory with an FG composes of discrete Si nanoparticles was proposed in 1996 [7]. This FG can reduce the charge loss in conventional FG devices. Si and Ge semiconductor nanoparticles have received attention as promising candidates to replace the conventional FG flash memory. However, the retention characteristics of these Si and Ge semiconductor nanoparticles are highly sensitive to the thermal process during device fabrication. These characteristics are influenced by defects and traps inside or on the surface of Si and Ge semiconductor nanoparticles [8, 9]. These defects and traps limit the application of these nanoparticles in NVM. In addition, memory devices with metallic nanoparticles offer better memory characteristics than those with semiconductor nanoparticles. Thus, metallic nanoparticles have been widely studied since 2003 [8, 10, 11].

Metallic nanoparticles improve data retention in memories than Si nanoparticles [12]. The work function is the minimum thermodynamic energy needed to remove an electron from a solid to a point in the vacuum immediately outside the solid surface. Metallic nanoparticles embedded in dielectric layer memories have several advantages, including high operation speed, good scalability, superior reliability, and diverse work functions [13]. Various metallic nanoparticles such as Au, Ag, Pt, and Al have been used as storage centers for NVM applications [13-16]. Among these nanoparticles, embedded AuNPs have been widely investigated because of their chemical stability, facile synthesis, and high work function of 5.10 eV [17-20].

AuNPs are embedded inorganic dielectric materials to form NVM devices based on a hybrid organic–inorganic system. Among organic dielectric materials, polymethylmethacrylate [21], polydimethylsiloxane [22], and polystyrene-block-poly(4-vinylpyridine) (PS-b-P4VP) [23] have been used in memory devices. Meanwhile, polymethylsilsesquionxane (PMSSQ) is an organic–inorganic (hybrid) material that combines the desirable physical characteristics of both organic and inorganic materials. PMSSQ is a distinctly excellent dielectric material because of its low dielectric constant (~2.7), low moisture absorption, excellent thermal stability of up to 500 °C, and excellent mechanical strength (1.9 GPa hardness, 12 GPa modulus) [24, 25]. This hybrid organic–inorganic system has emerged as a structure of memory devices in next-generation electronics and optoelectronics. The system, which displays a “floating” AuNP layer in the middle of the organic semiconducting material, can create bi-stable properties [26]. Electrical bi-stability is a

phenomenon in which a device exhibits two states of different conductivities at the same applied voltage. This behavior is ideal for switching and storage applications and has been proven in both inorganic and organic materials [27].
This chapter covers recent developments in the fabrication of AuNP thin films and their applications in NVM devices. Theoretical knowledge and typical conduction mechanisms of this hybrid memory device are also discussed in detail.

Gold nanoparticles (AuNPs)

"Soluble gold," which was discovered around the 5th or 4th century B.C. in China and Egypt, was used for both aesthetic and therapeutic purposes. The most famous example is the Lycurgus cup that was invented in the 5th to 4th century B.C. The presence of gold colloid causes the Lycurgus Cup to change color depending on the direction of light, that is, ruby red in transmitting light and green in reflected light. Gold colloid also played remarkable roles in the diagnosis of syphilis, heart and venereal problems, dysentery, epilepsy, and tumors in the middle ages [17].
Modern scientific evaluation of gold colloid began when AuNPs were first investigated in the 1850s by Michael Faraday, which then motivated nanomaterial investigation. In 1974, Japanese researcher Taniguchi first used the term "nanotechnology" to refer to the ability of engineering materials produced at the nanometer scale [28]. Researchers in the 20th century investigated intensively the fundamental and applied aspects of AuNPs because of the quantum size effect [29, 30]. The majority of the references and review articles in the 21st century reported promising applications of AuNPs in various fields, including electronics, optoelectronics, catalysis, and biology [13, 17, 31, 32]. All of these applications are dependent on the properties of AuNPs.

Properties of AuNPs

Nanoparticles have drawn substantial attention because of their small size (1–100 nm) and corresponding large surface-to-volume ratio. Among the noble metallic nanoparticles, AuNPs have been used in a broad range of applications, including material science, catalysis, biomedicine, and quantum dot technology, because of their attractive optical properties in photonic device fabrications, photothermal properties in sensing organic and biomolecules, and electrical properties in charge storage systems [17-20].
The unique optical properties of AuNPs with varying sizes and structures are due to the illumination of surface plasmon resonance (SPR) [19, 33]. SPR is a resonant oscillation of conduction electrons at the interface between a negative and positive permittivity material stimulated by incident light. Resonance condition is established when the frequency of incident photons matches the natural frequency of surface electrons oscillating against the restoring force of positive nuclei. The strongly enhanced SPR of noble AuNPs at optical frequencies renders them excellent in scattering and absorbing visible light [19, 33, 34].
The SPR properties of AuNPs are promising in biochemical sensing and detection, medical diagnostics, therapeutic applications, and biomedical applications because of their biocompatibility and non-toxic properties [17]. Moreover, the use of AuNPs has become one of the greatest recent successes in photothermal therapy. Such photothermal properties are formed when AuNPs are excited with a specific band light (mainly infrared), and the excited state releases vibrational energy in the form of heat [19]. This heat is widely used in photothermal therapy to kill targeted cells.
The physical and chemical properties of AuNPs can be modified by changing their composition and size [35]. Figure 7.1 shows the color difference of particle solutions with varying sizes of spherical

AuNPs [36]. The memory effect of the device can be controlled by tuning the density and distribution of AuNPs [21].

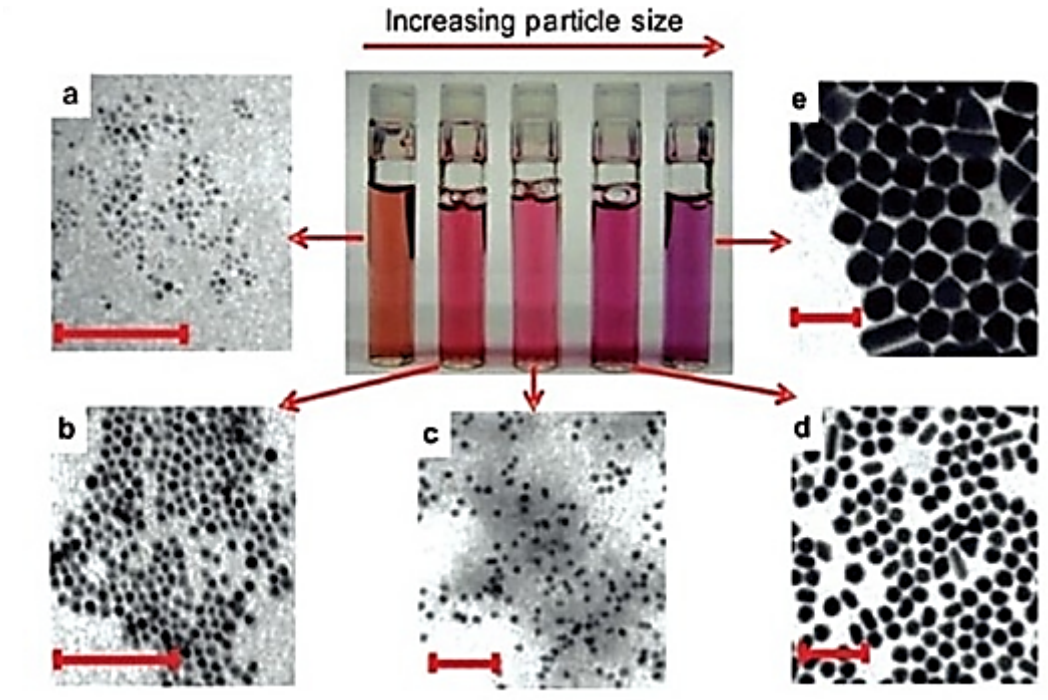

FIGURE 7.1
Photographs of aqueous solutions of gold nanospheres as a function of increasing dimension. Corresponding transmission electron microscopy images of the nanoparticles are shown (all scale bars 100 nm) [36]

AuNPs provide another excellent electrical property by acting as charge trapping elements in NVM devices. Charge carriers are stored in AuNPs when voltage is applied across the electrode of a device [37]. AuNPs exert a promising memory effect because of their chemical stability, facile synthesis, and high work function (5.01 eV) [20]. However, the distribution of AuNPs is a crucial factor in the fabrication of memory devices.

Formation methods of AuNPs on substrates

AuNPs are in the form of thin film in most electrical and electronic devices. The main challenges in the formation of AuNPs on substrates are the achievement of uniform size and shape of nanoparticles, uniform distribution, and adhesion of AuNPs on the substrate. Controlling the size and structure of AuNPs is technologically important because of the strong correlation between these parameters with physical and chemical properties. Therefore, specific control of shape and size is often difficult and can be varied by different methods. Many methods have been used for the formation an AuNP layer on a substrate; these methods include self-assembly, Langmuir–Blodgett (LB) layer, heat treatment of gold thin film, and direct synthesis onto a template-based

surface. Each method is described accordingly in the later section, and the advantages and disadvantages of each method are listed in Table 7.1.

TABLE 7.1
Fabrication methods to produce AuNPs on substrates

Method	Advantages	Disadvantages	Published works using the method
Self-assembly	- Highly monodispersed and organized AuNPs can be produced on the functionalized substrate	-Costly and time consuming -Polymeric linker molecules cannot be removed from the surface and will eventually affect the memory properties	[38-44]
Langmuir–Blodgett	- High degree control of AuNP density and order by monolayer manipulation	- Problem in controlling the homogeneity of AuNP arrays	[45-48]
Heat treatment of gold thin film	- Simple and common - AuNP size and distribution can be tuned by changing physical conditions such as temperature, temperature gradient, and time spent.	- High temperature processes cause metallic contamination due to diffusion of metal atoms into polymeric layer -Difficult to control nanoparticles size and packing density - Too thick gold layer causes non-uniform dispersion and enlargement of clusters	[13, 31, 49-51]
Template-based approach	-Interparticle spacing between AuNPs can be controlled by template size. - Size and distribution of AuNPs can be tuned by template formation.	-Formation of AuNPs is not well distributed if the template is not well prepared	[52-58]

Self-assembly method

Self-assembly method involves the assembly of nanoparticles via absorption or spontaneous formation on the surface of a substrate. To create a stable layer, AuNPs possess a functional group that has a strong affinity to anchor the substrate. Self-assembly of AuNPs has different types, such as the self-assembly of functionalized AuNPs on a substrate [38, 39], the self-assembly of AuNPs on

a modified substrate [38, 40-42], and the self-assembly of functionalized AuNPs on a modified substrate [43, 44].

The self-assembly of functionalized AuNPs on a substrate is employed by utilizing the chemical interaction between AuNPs and the substrate surface. For example, organic molecules containing thiol (–SH) or amine ($–NH_2$) are the capping agents that can be adsorbed on the AuNP surface and then form a well-organized self-assembly monolayer on the substrate [38]. The size, shape, and interparticle separation of these uniform size distribution particles are controlled by the nature of the capping agents. During the processing steps, the capping already exists during metal salt reduction and surfactant presence in the solution. Therefore, highly monodisperse and organized AuNPs can be formed on the substrate through this self-assembly approach [39].

The self-assembly of AuNPs on a modified surface substrate involves the functionalization of organic terminal functional groups' materials on a substrate that is later used to immobilize AuNPs on it. For instance, metallic nanoparticles such as Au, Ag, and Pt can be attached to various thiol- and amino-terminated organosilane layers. A layer of *p*-aminophenyl trimethoxysilane (APhTS) and 3-mercaptopropyl trimethoxysilane (MPTS) films were used to immobilize AuNPs on Si substrates and Si-based device was formed [40]. A schematic of the covalent binding of AuNPs to a silicon oxide surface via MPTS and APhTS is presented in Figures 7.2(a) and 7.2(b), respectively. MPTS is a thiol-terminated organosilane molecule that covalently binds to AuNPs. In addition, the terminal amino groups of APhTS have an affinity to hydrogen bond with neighboring molecules. However, this approach often leads to the aggregation of organosilane molecules and formation of disordered multilayer films.

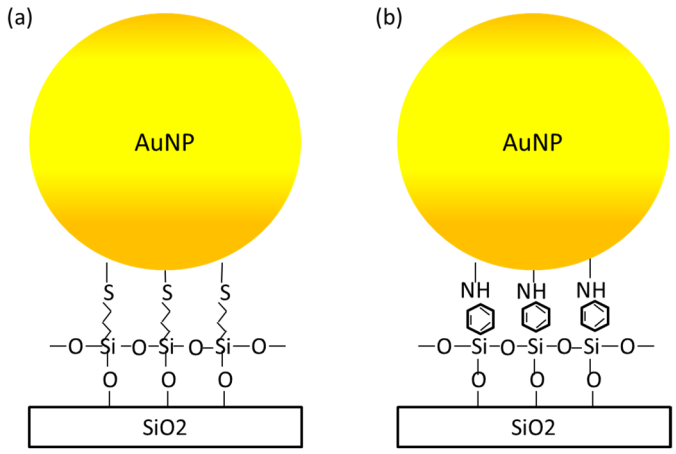

FIGURE 7.2
Schematic of a AuNP attached to a (a) MPTS-coated silica surface and (b) APhTS-coated silica surface

Some studies have also performed the reproducible self-assembly of AuNPs attached to a 3-aminopropyltrimethoxysilane (APTMS)-modified substrate via spin coating [38, 41]. The schematic of this method is shown in Figure 7.3. AuNPs fabricated on APTMS pre-modified fused silica and silicon oxide by spin coating obtained high density and uniformity in AuNPs as observed by other authors [38, 41].

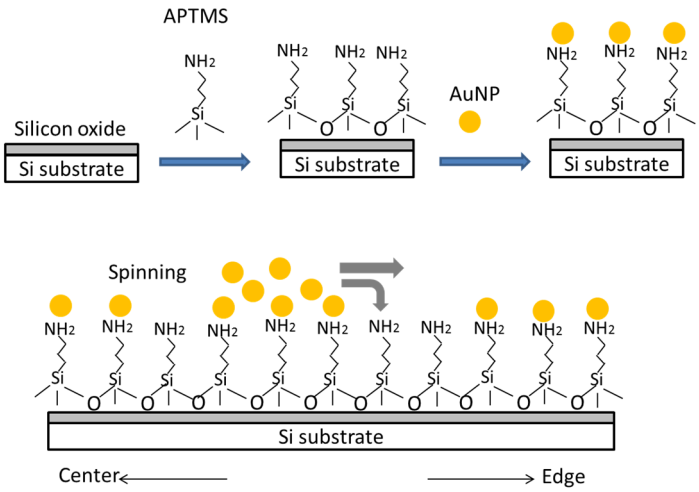

FIGURE 7.3
Schematic of the self-assembly of AuNPs on APTMS-modified substrate

However, the parameters in spin coating must be optimized to achieve a uniform distribution of AuNPs. This is due to the centrifugal force during spin coating may cause the liquid to drain radically off the edge of the substrate until solvent evaporation leaves a solute-rich liquid. The solute-rich phase is too viscous to flow readily, ultimately forming large concentric arrays of liquid droplets [39]. The liquid droplet contains imperfect agglomerate AuNPs that can ruin electrical properties when used in devices [39].

Apart from APhTS and MPTS, aminopropylsilatrane (APS) and 3-aminopropyltriethoxysilane (APTES) as chemical linkers were developed as another controlled strategy to bind AuNPs to glass slides or optical fibers [42]. Figure 7.4 shows the procedure for anchoring AuNPs on (a) APTES- and (b) APS-modified glass slides or optical fibers. In their study, APS was extremely resistant to hydrolysis and polymerization at neutral pH, such that it allows simple laboratory preparation. However, APTES is highly sensitive to moisture. This condition causes the agglomeration and polymerization of AuNPs on the glass substrate during deposition, which can be a serious problem when AuNPs are used as linkers in sensor applications.

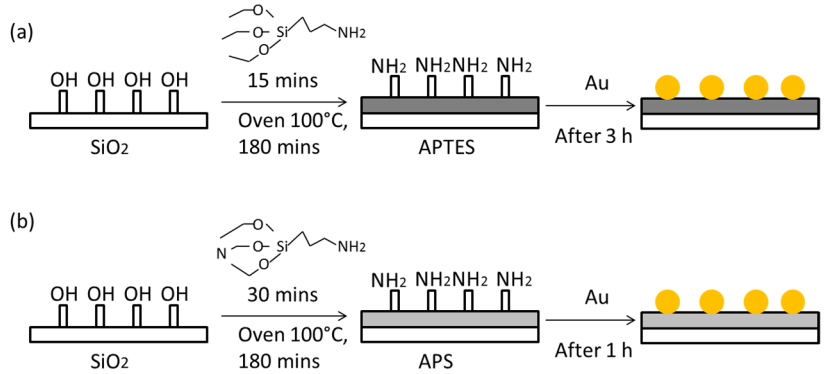

FIGURE 7.4
Illustration showing the procedure for anchoring AuNPs on (a) APTES- and (b) APS-modified glass slides or optical fibers

A study about the self-assembly of functionalized AuNPs on a modified surface substrate was reported before [44].The group synthesized and covalently immobilized 11-mercapto-1-undecanol (MUD) functionalized AuNPs on a hydroxyl-terminated Si substrate using gantrez polymer as a surface modifier [44]. A schematic for the distribution of AuNPs is shown in Figure 7.5.

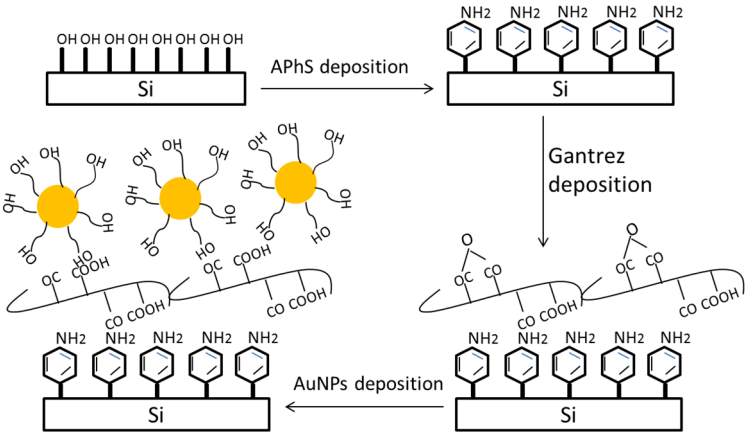

FIGURE 7.5
(a) Schematic of immobilization of MUD-capped AuNPs on a hydroxyl-terminated Si surface

Besides that, the assembly of AuNPs on a modified glass substrate surface was also reported [43]. During the preparation process, a glass substrate was cleaned thoroughly to ensure the maximum exposure of OH groups on the surface prior to immersion in siloxane solution for surface functionalization. This strategy provides the best possible surface for AuNP functionalization through absorption. This modified glass surface provides chemical groups that can bind the colloidal particle either covalently or through electrostatic interactions. However, this method of AuNP deposition on the substrate is costly and time consuming. The functionalization of the substrate with polymeric linker molecules attached to the Si substrate cannot be removed from the surface, eventually affecting the current conduction of electronic devices.

Langmuir–Blodgett method

The LB method can control the deposition of nanoparticles over a large area. This method is almost similar to the "surface tension-driven" method, which has also been used for the direct assembly of nanoparticle layers. The nanoparticles can be immobilized at the air–water interface within a "carrier" monolayer [46].
Figure 7.6 illustrates the typical steps to obtain the Langmuir monolayer at the air–water interface of the substrate. In this method, amphiphilic molecules such as dodecanethiol-capped AuNPs that consist of hydrophilic and hydrophobic moieties are dissolved in an organic solvent such as chloroform. The monolayer, with a thickness in the molecular scale, can be formed by controlling the surface pressure when dipping the substrate into the solution. The magnitude of intermolecular interactions between the molecules is enhanced with increasing pressure. The chemical designs of the hydrophilicity and hydrophobicity of the component molecules are important to obtain a stable monolayer at the air–water interface [45].

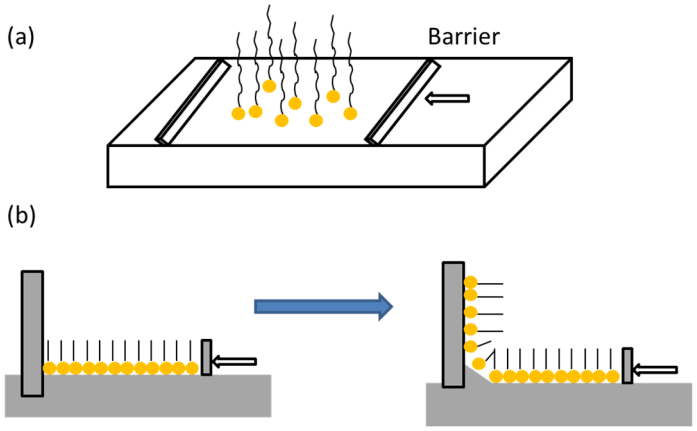

FIGURE 7.6
Langmuir–Blodgett technique for the fabrication of nanoscale thin-film structures. a) Langmuir monolayer at the air–water interface. An amphiphilic molecule has a hydrophilic head and a hydrophobic tail. Surface pressure can be controlled by moving barriers. b) Transfer of Langmuir monolayer onto substrate surface

An assembly of dodecanethiol-capped AuNPs on the substrate was performed by spreading the precipitates of dodecanethiol-capped AuNPs which was dissolved in chloroform. Then, the dodecanethiol-capped AuNPs settled onto the wafer after the solvent evaporated [59]. This LB film enables a high degree of control over the nanoparticle density and order because the monolayer can be manipulated prior to the assembly of particles on the substrate by producing thin and dense sub-layers. However, this method is complicated and cannot easily control the homogeneity of nanoparticle arrays [47, 48].

Heat treatment of Au thin film

AuNPs can be formed by heating a thin layer of gold film. Thin gold film layers of 1–5 nm are first deposited by e-beam evaporation and then annealed at an elevated temperature close to its eutectic temperature in an inert ambient gas to transform the thin gold film layer into nanoparticle structure. Heterogeneous nucleation from a liquid or gaseous phase and thin film dewetting cause AuNP formation in a gold thin film layer on a substrate under heat treatment. In heterogeneous nucleation, the film is initiated by the interaction between defects and film atoms. This process can be reacted by changes in physical conditions, such as temperature, temperature gradient, and time spent at high temperature [13, 49].
Thin film dewetting is a simple and common method used to fabricate nanoparticles. The driving force of this method is derived from the surface energy reduction of the thin film and the interface energy between the film and the surface. This process is accomplished through the relaxation of film stress and is limited by surface mobility. During thermal treatment, film atoms gain enough surface mobility, allowing the film to assemble into a stable state in which the film breaks into “nanoparticles” along the initial perturbation to reduce the elastic energy carried by the stress built in the film during deposition. However, nanoparticle formation cannot ensure that the layer forms discrete particles completely [49-51]. Size of AuNPs could be influenced by gold thin film layer thickness deposition reported [51]. In the study, an overly thick gold layer could enlarge clusters that are not well dispersed as shown in Figure 7.7.
The disadvantages of using heat treatment in the formation of AuNPs are the difficulty in

controlling nanoparticle size and packing density. In addition, the high-temperature process for producing AuNPs can be a source of metallic contamination because of the diffusion of metal atoms into the polymeric layer of the embedded structure [31].

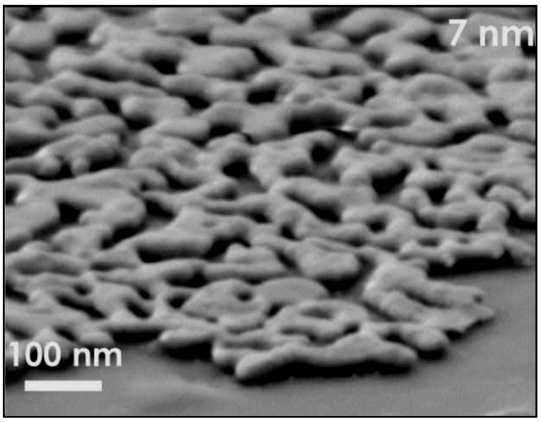

FIGURE 7.7
SEM images at 30° tiltof AuNPs deposited on a glass substrate for a 7 nm-thick gold thin film layer on a substrate [51]

Template-based approach

Although various fabrication approaches have been proposed in the latest nanofabrication area, the uniformity of AuNP distribution on a large area remains the main issue during fabrication. Therefore, researchers suggested the use of template-based substrates for well-controlled and high-density AuNP assembly over large areas to build high-performance devices [52-54].
AuNPs were formed by using ordered arrays of hemispherical nanowells as a template (Figure 7.8) [53]. The silica nanowells were formed in a sol–gel-derived silica film on a gold substrate using 500 nm-diameter polystyrene (PS) latex spheres. Two methods can be employed to form the nanowells. The first method involves doping of silica sol with PS spheres and spin coating the composite sol on the electrode surface. The second method involves spin coating an undoped silica sol on the surface before forming the monolayer of PS spheres. The PS spheres are then removed by soaking in chloroform to form silica nanowells on the gold electrode. The silica nanowells can be used as reduction sites for gold deposition. Thus, AuNPs are formed by the enlargement of the conductive domain located at the bottom of the nanowell template through electroless deposition, which involves immersing in a solution containing $HAuCl_4$ in the presence of the reducing agent NH_2OH. The size/microstructure of AuNPs can be controlled by changing the exposure time of electroless deposition [53].
The benefits of growing arrays of AuNPs using this approach are that the interparticle space between AuNPs can be controlled by the size of the template used to form the nanowell, the size and shape of resultant AuNPs can be controlled by the size and shape of the nanowell, and the silica support helps prevent the aggregation of nanoparticles as they begin to grow. However, the drawback of this method is that AuNP formation is not distributed uniformly across the entire substrate surface when nanowell formation is not well distributed (Figure 7.9), hence limiting their potential for memory device application.

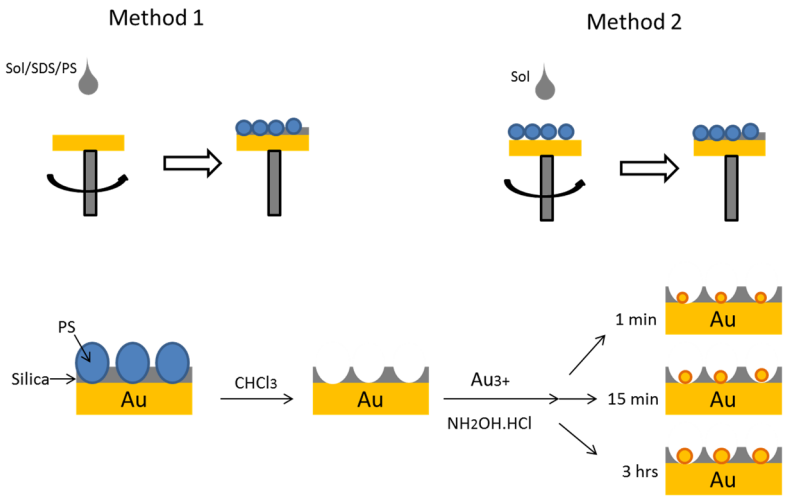

FIGURE 7.8
Schematic of AuNP formation using ordered arrays of hemispherical nanowells as template [53]

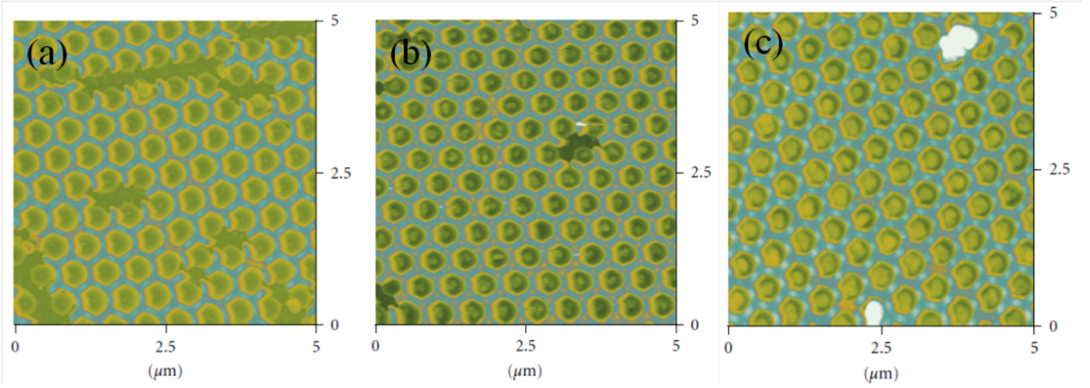

FIGURE 7.9
AFM images (5 μm × 5 μm) of gold deposited in silica nanowells grown by electroless deposition for (a) 1 min, (b) 15 min, and (c) 3h exposure times [53]

Another method of forming AuNPs using the template-based method was reported by Gupta et al. [54]. In their work, the substrate surface was modified with polystyrene-block-poly(2-vinylpyridine) (PS-b-PVP), which formed reverse micelle arrays as a template for AuNP deposition. The PS-b-PVP template was formed on the surface by spincoating *m*-xylene solutions. AuNPs were then deposited on the well-prepared template by incubating into $HAuCl_4$ solution; eventually, the polymer template was removed by O_2 plasma reactive-ion etching (RIE). The PS templates were exposed to O_2 RIE (50 mTorr, 50 W, 20 sccm O_2) for 120 s to remove the residual layer. Figure 7.10 shows the schematic for the formation of AuNPs with a micelle array template.

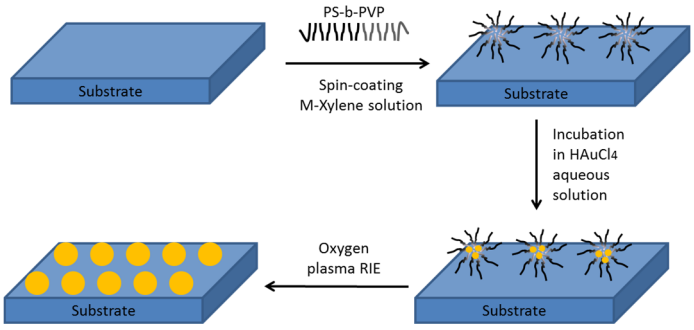

FIGURE 7.10
Schematic for the formation of AuNP arrays

Moreover, AuNPs were successfully formed on a seeded ZnO template using the low-temperature sacrificial hydrothermal growth technique (Figure 7.11) [52]. In their study, ZnO templates were annealed at various temperatures to tune the morphology of ZnO seeds. AuNPs were formed at the high energy sites of ZnO seed grain boundaries during the hydrothermal reaction in a bath containing 0.1 M zinc nitrate tetrahydrate ($Zn(NO_3)_2{\cdot}4H_2O$), 0.1 M hexamethylenetetramine ($C_6H_{12}N_4$), 0.01 M gold(III) chloride trihydrate ($HAuCl_4.3H_2O$), and 10 mL of acetic acid. The ZnO seed template dissolved into the hydrothermal reactive bath during the reaction because of the competitive reaction between Au and ZnO formations, which was attributed to the difference in Gibbs free energy (ΔG Au = −421.59 kJ/mol and ΔG ZnO = 16.08 kJ/mol). A negative ΔG value indicates a spontaneous process and, conversely, a positive ΔG indicates non-spontaneity; thus, the formation of AuNPs is favorable when a negative ΔG value is obtained. This hydrothermal reaction is an interesting synthetic protocol because it is low cost and environmentally friendly; moreover, this protocol allows uniform AuNP distribution, adjustable AuNP size, and large-area fabrication. The low substrate temperature enables this method to create various nanostructures on temperature-sensitive substrates [60].

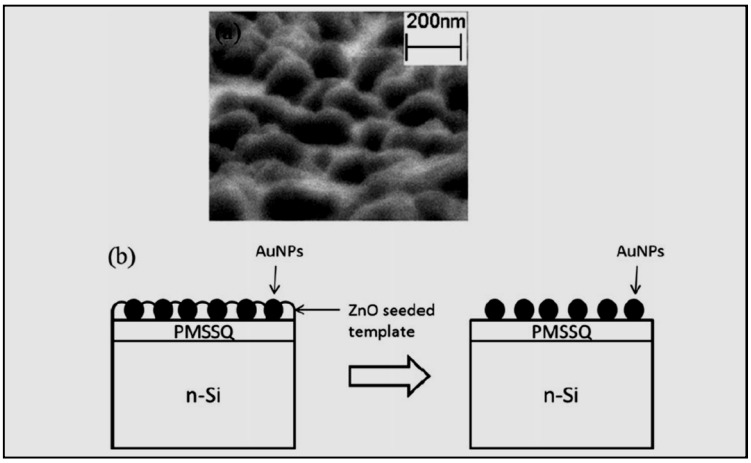

FIGURE 7.11
(a) FESEM image of AuNPs grown using the ZnO template. (b) Schematic of AuNP formation between the ZnO seed layer and the ZnO-seeded template by dissolution in an acidic hydrothermal reactive bath [52]

The size and distribution of AuNPs are influenced by template type. AuNPs can be grown not only on a ZnO template but also on an Al template by using the sacrificial hydrothermal method. In general, the size, shape, and distribution of nanomaterials depend on template type [57]. This basic theory is applicable in their study, in which the size and distribution of the AuNPs formed were confined by the template.

During a hydrothermal reaction, AuNPs nucleate on Al grain boundaries with high surface energy sites. The effect of annealing temperature for the Al template on AuNP formation was investigated. The grain size of Al templates increases with increasing annealing temperature because of ion diffusion. The grain boundary area between the Al template increases, resulting in the formation of large AuNPs with the increase in Al grain size. Meanwhile, a low AuNP area density can be observed with the formation of large AuNPs.

The duration of hydrothermal reaction may also affect the size and distribution of AuNPs [56]. This finding agrees with the result of Sanchez-Mendieta et al. [61] that nanoparticle size depends on reaction time. In their study, large nanoparticles were produced as the reaction time was prolonged because long hydrothermal reaction time increases the reduction of AuNPs via the diffusion of Au ions [61].

The size and distribution of AuNPs are also dependent on the concentration of hydrothermal precursor. For instance, the effect of $Zn(NO_3)_2$ concentration on AuNP formation accompanies the chemical reaction shown in Equation 1.

$$2Au^{3+} + 3ZnO \leftrightarrow 2Au + 3Zn^{2+} + 3O^{2-} \quad (1)$$

High concentration of $Zn(NO_3)_2$ provides more Zn^{2+} ions, causing the shift of the chemical reaction to the left, suppressing the formation of AuNPs to low area density, and producing a small size. However, overly high concentration of $Zn(NO_3)_2$ undergoes reduction with the reducing agent, causing an insufficient amount of reducing agent to react with $HAuCl_4$ to form AuNPs. Thus, excessive Au^{3+} ions are present in the hydrothermal bath. Hence, agglomerated AuNPs form when high concentration of $Zn(NO_3)_2$ is added into the hydrothermal bath.

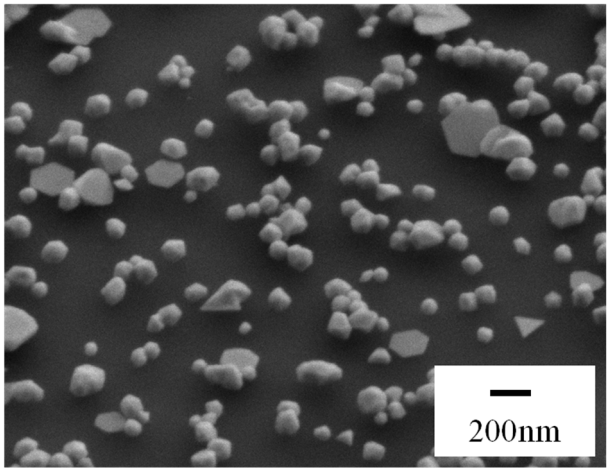

FIGURE 7.12
Morphologies of AuNPs with 0.10 M $Zn(NO_3)_2$ concentration [55]

As shown in Figure 7.12, triangular AuNPs formed on the sample probably because the hydrothermal bath contained complex functional compounds, including amine oxide, hydroxyl, and carboxylic groups, which affect the formation of nanoparticles with various shapes [55]. Moreover, the hydroxyl functional groups present in the precursor could facilitate the reduction process, interact with the surface of AuNPs, and stabilize these nanoparticles. Hence, a specific interaction between the precursor and the different surface planes of the AuNPs under ambient conditions can significantly favor the formation of triangular or hexagonal nanoparticles [62].

Non-volatile memory devices

Portable electronic products that require flash memories in the devices have become an important component of our daily life. NVM devices were first introduced in late 1960s, after which the market grew rapidly, especially that for FG device structures. The FG is the most prevailing NVM implementation and is widely applied in embedded memories. The FG structure was invented and organized into the primary technology necessary when built as a flash memory (Figure 7.13).

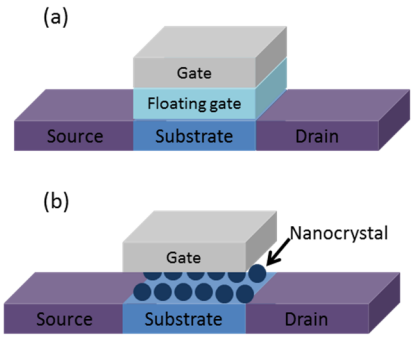

FIGURE 7.13
(a) Floating gate non-volatile memory structure. (b) Nanocrystal non-volatile memory structure

The shrinking of devices has evolved to meet the demand for product miniaturization. In such situations, the conventional NVM of the FG suffers from certain physical limitations, such as the insufficient tunneling oxide thickness from continuous scaling down of device structures. This condition causes serious reliability issue for memory applications because scaling down of device size induces significant leakage current and increases power consumption during reading and programming. Thus, flash memory devices with discrete charge trapping layers, such as nanoparticle-based memory devices, have been studied since the early 1990s. The layer of discrete nanoparticles is placed in mutually discrete crystalline nanoparticles or “dots” instead of a continuous material layer structure. These discrete nanocrystal memories were first suggested by IBM in 1995, and researchers found that these memories can potentially solve the problem of scaling down in the early 2000s (Figure 7.13(b)). In addition, nanoparticle memory has a two-bit-per-cell storage capability attributed to its discrete electron storage center. Thus, more data can be stored in one memory cell so that it readily increases memory density.
In discrete nanoparticle memory or nano-FG memory, semiconductor or metal nanoparticles are embedded as charge storage materials between the control oxide layer and the tunneling layer

instead of the continuous FG layers used in conventional flash memories. Nanoparticle charge storage offers several benefits. First, this type of device has the potential to use thinner tunnel oxides without sacrificing non-volatility when reducing the thickness of tunnel oxides, thereby lowering operating voltage and increasing operating speed. Second, the quantum confinement effect of small nanoparticles enhances the memory's performance of the FGNVM device. Third, the fabrication of nanoparticle memories is simpler and cheaper compared with conventional FG NVM.
The first proposed flash memory with an FG was made with Si nanoparticles [7]. Metal nanoparticles have been recently proposed to improve data retention because metal nanoparticle memories have greater work function than Si [12]. Metal nanoparticle memories possess several advantages, including small operating voltage, high operation speed, good scalability, superior reliability, and favorable endurance characteristics [13].
Among the various types of metal nanoparticles (e.g., Au, Ag, Pt, and Al) that serve as storage centers for NVM applications, AuNPs exert the best memory effects so far because of their chemically stable characteristics and wide work function (Table 7.2). The high work function of AuNPs provides a high confinement barrier for the retention mode and a small barrier for the programming and erasing modes. Although the work function of Pt is higher than that of Au, AuNPs are more widely used than PtNPs because Pt is a rare metal (< 0.003 ppb in the earth's crust) with a higher price than Au [63]. The rough world market price for Pt is currently at $38902/kg, whereas that for Au is $38130/kg [64, 65].

TABLE 7.2
Work function of various materials, in units of electron volt (eV)

Metal	Work function (eV)
Pt	5.6
Au	5.1
Ag	4.4
Al	4.3
Si	4.7
Ge	4.8

NVM devices based on a hybrid organic–inorganic system have emerged as a structure for memory device applications in next-generation electronics and optoelectronics. This hybrid organic–inorganic system is formed by mixing inorganic metallic nanoparticles into organic materials. The system has a “floating” metallic layer formed by disconnected nanoparticles in the middle of the organic semiconducting material, thereby creating bi-stable properties [26]. This electrical bi-stability is a phenomenon in which a device exhibits two states of different conductivities at the same applied voltage. This behavior is ideal for switching and storage applications and has been proven in both inorganic and organic materials [27]. Some nanomarket firms are looking in to the coexistence of organic-based transparent electronic materials and inorganic metallic nanoparticles in the device structure to upgrade the technology for transparent digital signage in the near future.

Hybrid organic–inorganic non-volatile memory device

Organic materials are promising candidates for future molecular-scale device applications. For example, resistive switching could be achieved by depositing a layer of Al nanoparticles between two organic layers [27]. The distribution of nanoparticles can be controlled in these devices because the deposition of the nanoparticles and the organic layer are independently controlled.
Some works reported the electrical behavior of metal–insulator–semiconductor (MIS) structures that were fabricated on Si substrates and used organic thin films as dielectric layers [1, 66-68]. Memory window was attributed to the charging and discharging of nanoparticles from the gate electrode in Al/pentacene/Au nanoparticle/SiO_2/p-Si structure. A maximum memory window of 2.5 V was achieved by scanning the applied voltage between 9 V and −9 V. This hybrid organic–inorganic NVM is currently applied on thin-film, transparent, or even flexible electronics [67].

Memory properties of AuNP-embedded organic insulator

The charge-trapping behavior of an AuNP-embedded organic insulator memory device can be determined by electrical measurements, such as capacitance–voltage (*C–V*). *C–V* measurement is carried out to verify the memory effect of devices. A hysteresis window is obtained in a forward and reverse sweep. The *C–V* plot indicates when a significant amount of charge trapping occurs in the device. The charge storage (electrons/holes) capacity per particle in the device can also be calculated via the flat-band voltage (ΔV_{FB}) value measured by the *C–V* results. Electrons/holes injected from the active layer to the charge storage layer through the dielectric layer are related to the negative/positive voltage bias applied. The charge storage occurs with the electron carriers when a negative voltage is applied, whereas the hole carriers occur when a positive voltage is applied to the sample (Figure 7.14).

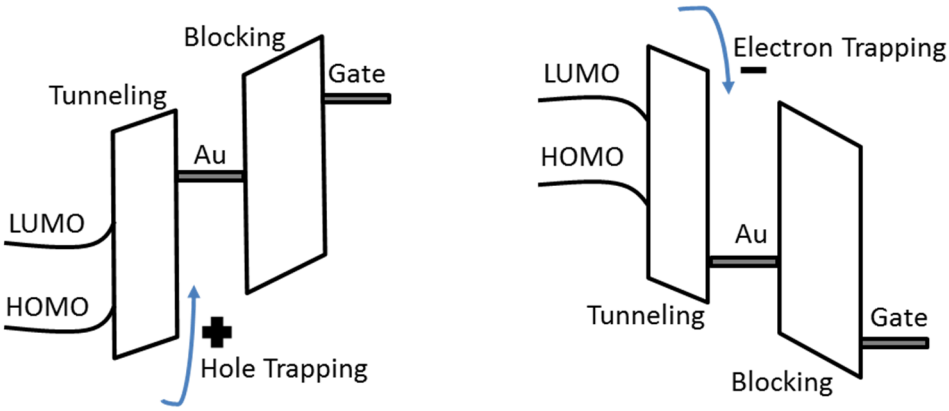

FIGURE 7.14
Energy band diagrams of the memory transistor at hole-trapping mode and electron-trapping mode

In current–voltage (*I–V)* measurement, the threshold voltage (V_{th}), I_{on}/I_{off} ratio, and conductance mechanism of the device can be characterized through the *I–V* curve. V_{th} is the minimum voltage level that produces a given effect, result, or response, such as detection, activation, or operation. V_{th} is also known as the lowest voltage needed to switch a transistor from a blocking state to a conducting state to turn “ON” the device. An abrupt increase in the current that switches the lower

conductivity state to the higher conductivity state occurs in V_{th} of the *I–V* curve. The I_{on}/I_{off} ratio, another parameter that can be derived from the *I–V* curve, is defined as the ratio for the on-state current and off-state current in the device. The best properties obtained across nanoparticle-embedded memory devices are listed in Table 7.3, with V_{th}< 6 V and a typical I_{on}/I_{off} ratio of 10^4 – 10^9. For further property enhancement, V_{th} could be reduced from more than 10 V to below 4 V. The > 2V memory window under a10 V bi-directional voltage sweep is also of interest.

TABLE 7.3
Desired memory properties for embedded nanoparticle structure memory devices

Electrical property	Value	Reference
V_{th}	< 6 V	[25, 52, 69, 70]
I_{on}/I_{off} ratio	10^4–10^9	[52, 71, 72]
Memory window	> 2 V	[70, 73]

In *C–V* characteristics, a device with embedded nanoparticles that exhibit significant hysteresis window shows the storage of charge in the nanoparticles to gain the memory effect [25, 46]. For instance, the typical properties for NVMs with and without AuNPs that were fabricated by a unique laser irradiation method was investigated [74].The charge trapping properties of electrons and holes in AuNPs (average 8 nm diameter) with $1 \times 10^{12}/cm^2$ area density embedded in MIS on p-type Si (100) substrates are shown in *C–V* characterization. The best flat-band voltage shift (or memory window) of 1.9 V was revealed for the sample with AuNPs after the voltage was swept from +8 V to –8 V. The appearance of memory window indicates the existence of trap sites occupied by carriers. Higher applied sweep voltage leads to a wider hysteresis window. No hysteresis was obtained in the device without AuNPs embedded, indicating that the AuNPs contributed to charge storage. However, negligible hysteresis was produced after the gate voltage was swept from +7 to –7 V. This result indicates that some trapped sites remain in the gate oxide layer or minimal interface states exist at the substrate/oxide layer and oxide layer/AuNPs even though the AuNPs serve as charge traps [74]. The origin of these traps is related to the type of substrate, oxidation (ambient and temperature), wafer orientation, or ionic impurities [75].

The capacitance characteristics of AuNPs embedded on metal–oxide semiconductor (MOS) capacitors with Al_2O_3 control oxide layers were investigated [76]. The capacitance versus voltage curves obtained for a representative MOS capacitor embedded with AuNPs (5 ± 0.5 nm) having a density of 2.86×10^{16} m^{-2} and synthesized by the colloidal method exhibited a large flat-band voltage shift because of the stored charge in the AuNPs. The normalized capacitance versus voltage curve measured at a frequency of 1 MHz was obtained. A flat-band voltage shift of 4.3 V was obtained when the voltage was swept from −7 to 7 V, and vice versa. The *C–V* curve taken for the reference MOS capacitor without any AuNPs (as reference sample) exhibited negligible hysteresis (0.1 V), which agrees with the results obtained by [74].

In addition, the clockwise hysteresis and the rightward shift of the flat band voltages observed from the *C–V* curves implied that electrons were trapped in a floating gate layer and these trapped electrons were originated from the top electrode and also the subsequent extraction of electrons from the AuNPs situated in the inversion region to the electrode. Moreover, the clockwise nature of the hysteresis (for a p-type semiconductor) is usually associated with ion drift or polarization of the insulator [46].

Hysteresis characteristics are also dependent on the voltage sweep range [23, 76-78]. The *C–V* characteristics of AuNPs embedded on a MOS capacitor were examined in three sweep ranges. The hysteresis window of the flat-band voltage shift widened when the sweep voltage range was

broadened. The flat-band voltage also shifted toward a positive voltage range when the voltage sweep range was widened because of the sweeping of the gate voltage from the accumulation in inversion regions.

The magnitude of ΔV_{FB} is dependent on the voltage sweeping range was reported by Leong et al.. The *C*–*V* hysteresis window increased from −0.19 V to −0.34 V and to −0.68 V upon increasing the operational bias from ±3V to ±4 V and to ±5 V, respectively. This change indicates an increase in charge injection toward the memory devices [79].

Besides that, the effect of AuNP loading on the memory effect was studied by Leong et al. At an operating voltage of ± 5 V, the *C*–*V* hysteresis window broadened from −0.68V to −1.47V and to −1.58V with increasing AuNP concentration (corresponding to 0.1, 0.2, and 0.3 molar ratios of $HAuCl_4$ per P4VP unit, respectively). This result indicates the occurrence of strong carrier trapping with increasing AuNP concentration. Conversely, the application of a pulse voltage of −5 V led to an injection of electrons from the top gold electrode, resulting in a positive V_{FB} [23].

The charge storage capacity per nanoparticle can also be calculated through the flat-band voltage value measured from the *C*–*V* characterization [52, 58, 80]. Equation 2 shows the calculation of charge storage capacity per nanoparticle. Flat-band voltage shift (memory window width) ΔV_{FB} is calculated for a single electron (n = 1) confined in a nanoparticle:

$$\Delta V_{FB} = \frac{nq d_{nanoparticle}}{\varepsilon_{PMSSQ}}\left(t_{gate} + \frac{1}{2}D_{nanoparticle}\right), \quad (2)$$

where *n* is the number of charges (electrons/holes) per single nanoparticle, *q* is the electron charge magnitude, $d_{nanoparticle}$ is the area density, t_{gate} is the thickness of the control gate (PMSSQ), $D_{nanoparticle}$ is the nanoparticle diameter, and ε_{PMSSQ} is the PMSSQ dielectric constant. From Equation 2, the stored charge density can be calculated by the memory window width obtained from the *C*–*V* curve. Meanwhile, the area density and nanoparticle size can be analyzed from the morphological analysis of the FESEM images. Nanoparticle size is directly proportional to the charge stored per nanoparticle through Equation 2. The amount of stored charge per single AuNP is also inversely proportional to the area density of AuNPs in the sample.

For example, in the work of AuNPs embedded in the PMSSQ memory device obtained a flat-band voltage in the *C*–*V* measurement. The number of stored charge per single AuNP was calculated by using the observed ΔV_{FB} of 3.6 V together with 90 nm particle size and 2.7×10^{13} m^{-2} area density on the basis of Equation 2. The amount of stored charges per single AuNP calculated was∼54 in the memory device [52]. In another work, 15 charges were trapped in each AuNP formed using the self-assembly monolayer of AuNPs, with an average diameter of 5 ± 0.5 nm and a density of 3.2×10^{11} cm^{-2}. The nanoparticles were embedded into the aluminum oxide (Al_2O_3) gate dielectrics that acted as trapping elements [81]. However, the charges trapped per AuNP in the work by [81] were lower than those in the work by [52]. In fact, the stored charge per single AuNP is influenced by the size and area density of AuNP.

In terms of the shape that can be formed in the *I*–*V* characterization, the S-shaped or N-shaped characteristics are commonly obtained in studies. Both nonlinear *I*–*V* curves exhibit a sudden switching, leading to the transition from a lower conducting state to a higher conducting state. Some differences in these two shapes of curves can be observed. When the curve exhibits an asymmetrical behavior, the device is erased, writes voltages in the opposite polarity, and assumes an N-shaped *I*–*V* characteristic. When the curve exhibits a symmetrical behavior, all functions can be performed with a single polarity and show the same characteristic (i.e., S-shaped *I*–*V* characteristic) in the negative voltage region. Another type of curve behavior is the O-shaped *I*–*V*

characteristic, in which the hysteresis loop is within the *I–V* characteristics, with no sudden switching due to an abrupt increase in current at a specific voltage [82, 83].

The memory effect was observed [57], who reported that electrons could be stored when AuNPs that are dispersed randomly in an insulating PMSSQ layer capture electrons that are injected from the electrodes. The memory device with an Au/PMSSQ/AuNPs/PMSSQ/Al structure showed the lowest increment in an abrupt current of 2.4 V, which is a particularly interesting electrical property, because only a low voltage is required to turn "ON" a memory device.

In the *I–V* characteristic, different types of electrode can affect the properties of the device. For instance, the voltages of two types of electrode (Au and Al) were compared at the V_{th} of the devices. Figure 7.15(a) shows MIS-A (structure with Au electrode), and Figure 7.15(b) shows MIS-B (structure with Al electrode). Figure 7.16 shows the result in which the Au-electrode MIS device is more favorable because of its lower V_{th} value at ~5.6 V than the Al-electrode MIS device, which is~13.6 V [69]. This result is explained by that the lower programming voltage is a better choice for memory device fabrication. The state (programmed or erased) of the MIS device can be read by detecting the difference in on-current and off-current. In this work, I_{on}/I_{off} ratios of ~10^2 and ~10 were achieved for MIS-A and MIS-B, respectively.

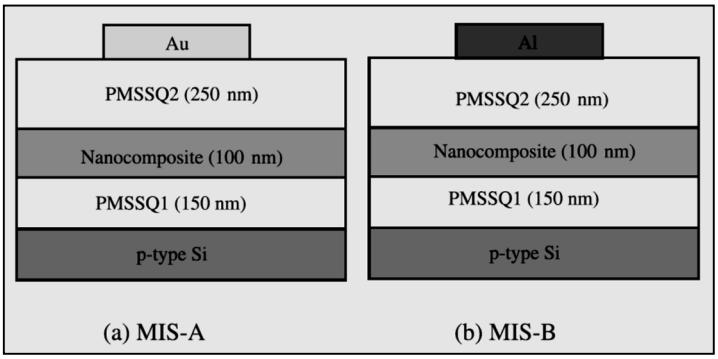

FIGURE 7.15
Cross sectional structure of the three fabricated MIS devices as NVM, (a) MIS-A and (b) MIS-B [69]

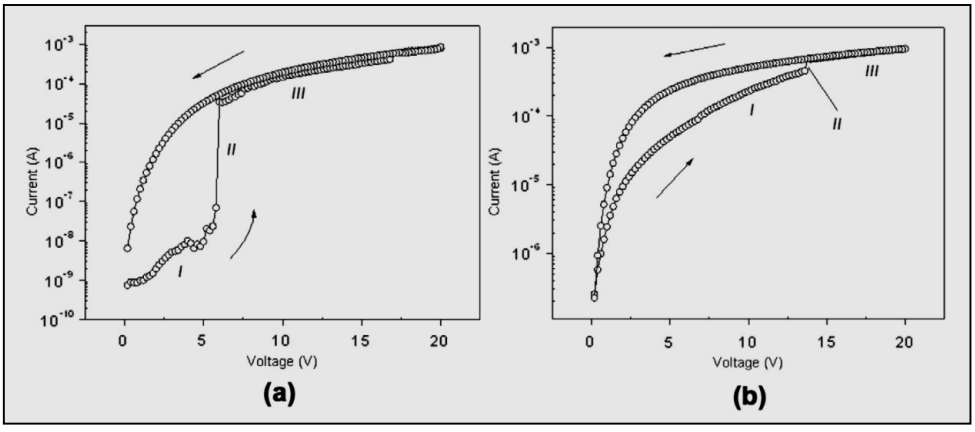

FIGURE 7.16
I–V characteristics of MIS. (a) MIS-A and (b) MIS-B on a semi-log scale [69]

The highest I_{on}/I_{off} ratio (10^9) as mentioned in Table 7.3 was obtained in an NVM device based on the AuNP-incorporated poly(9-vinylcarbazole) (PVK) film [84]. In their study, the weight ratio of AuNP/PVK was varied. The AuNP/PVK weight ratio of 0.2 obtained the highest I_{on}/I_{off} ratio because the large amount of AuNPs enhanced the properties of the device. However, PVK contained some defects of shallow-level energy states, which may act as electron traps [84].

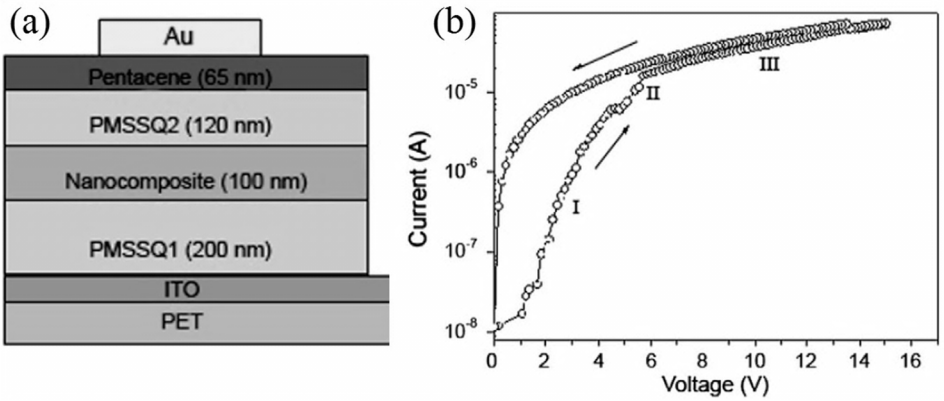

FIGURE 7.17
(a) MIS device with structure Au electrode/65nm Pentacene/120nm PMSSQ 2/100 nm nanocomposite mixture/200 nm PMSSQ1/ITO coated PET; (b) *I–V* characteristics of MIS device on a semi-log scale [25]

An optically transparent and flexible MIS memory device with a structure of Au/65 nm Pentacene/120 nm PMSSQ2/100 nm nanocomposite mixture/200 nm PMSSQ1/ indium–tin oxide (ITO)-coated polyethylene terephthalate (PET) was produced as shown in Figure 7.17(a) [25]. *I–V* plot of the transparent and flexible device showed the presence of hysteresis and V_{th} at 6.6 V when the voltage was swept from 0 to 15 V, and vice versa. During the forward voltage sweep, some current instability occurred before reaching the V_{th} because the current was trapped at the interfaces. In the *I–V* plot in Figure 7.18 (b), three distinct regions(I, II, III) were identified, the conduction mechanisms of which are explained below.

The observed *I–V* relationship is described as $I \propto V^n$, and the fitted slope of a double log plot determines the *n* value of log $I \propto n$ log V. The current state of the memory device initially remained low (high-resistance state, HRS) but gradually increased with increasing applied voltage. The abrupt increment in current was sensed at V_{th}, switching to low-resistance state. Thus, during the first sweep from 0 V at region I, the thermionic emission (TE) current conduction occurred at a low voltage, which is related to the thermally generated electrons, because TE is a process by which heat induces the emission of electrons across a barrier. However, the curve in region I can be fitted by Schottky and Poole–Frenkel emissions because electrons are possibly transported over the ITO–PMSSQ interface via Schottky emission (SE) and Poole–Frenkel (PF) emission in the 250 nm-thick porous silicate PMSSQ. Thus, electrons from ITO are transported across the barrier by thermionic effects via field-assisted lowering at the ITO–PMSSQ interface, combined with the Schottky and Poole–Frenkel emission effect. The results agree with the findings by Aw et al., who built a metal/dielectric/metal memory device structure that consisted of a Au electrode/200 nm Parylene-C/ 20 nm AuNPs/100 nm Parylene-C/ITO-coated PET [85].

With the increase in bias to V_{th}, the current in region II with the slope *n* became greater than 2 ($n > 2$), indicating that a typical trap-limited space-charge-limited current (SCLC), also known as trapped

charge limited current (TCLC) conduction mechanism, exists. In this region, the trap sites on the AuNPs were filled with electrons, and an abrupt increase in current was observed in the *I–V* measurement. After all the traps on the AuNPs were filled, region III switched in conduction mechanism following the trap-free SCLC, with an *n* of approximately 1.5 ($n \approx 1.5$), which obeys the Langmuir–Child law for SCLC rather than the predicted slope for SCLC in the bulk from the Lampert–Rose model of $n \approx 2$.

Another group also studied the conduction mechanism of a PS with AuNP bistable memory structure through *I–V* characterization [86]. The *I-V* plot in the study shows that the device switches from a low-conductivity state to a high-conductivity state upon application of an external electric field. The current transition exhibited a narrow voltage range, which caused an abrupt increase in current. This mechanism is schematically depicted in their work. At low voltage, the current was due to the thermally generated free carriers, which exhibited a linear voltage dependence. At a higher applied electric field, the carriers injected into the dielectric were from a thermionic process across the barrier. At the last stage with the highest applied voltage, the traps were completely filled, and the *I–V* characteristics followed the trap-filled SCLC model. Schematic band diagrams for the transport mechanism of PS+AuNP bistable memory structure are shown in Figure 7.18. Region I exhibits a thermally generated carrier conduction, region II shows the presence of traps, region III shows nearly filled traps, and region IV illustrates completely filled traps.

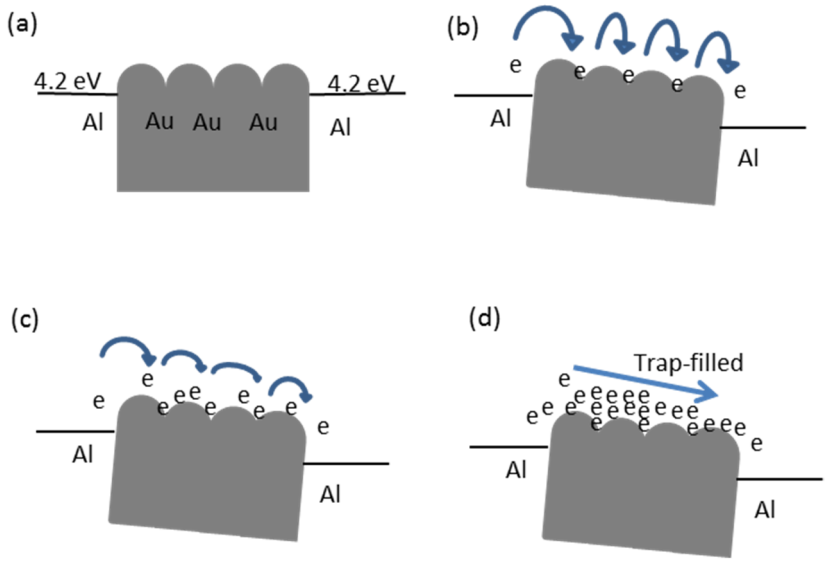

FIGURE 7.18
Schematic band diagrams for the conductance mechanism of trapped filled space-charge limitation conduction. (a) Region I: thermally generated carrier conduction, (b) region II: with traps, (c) region III: nearly filled, and (d) region IV: traps filled

Table 7.4 summarizes the memory characteristics of the *C–V* and *I–V* measurements of embedded AuNP memory devices. An excellent NVM device should attain the properties of low power consumption, sufficient memory window, and superior reliability in both *I–V* and *C–V* characteristics. Lower V_{th} value in the memory characterization is favourablebecause lower current is needed to switch on a memory device so that only low power consumption is needed. A higher I_{on}/I_{off} ratio value is also preferable in an NVM device because of the excellent electrical bistability

that comes with this property. As mentioned above, developments in memory devices should attain memory properties with a V_{th} of less than 6 V, I_{on}/I_{off} ratio in the range of 10^4–10^9, and memory windows greater than 2 V. Nevertheless, some of the devices failed to attain this benchmark. The conduction mechanism of the memory device, as obtained through the *I*–*V* characteristics, is summarized in the Table 7.4.

TABLE 7.4
Summary of memory characterization for embedded AuNP memory devices

Device structure	Description of *I-V* characteristics	Description of *C-V* characteristics	Conducting mechanism	Reference
Au electrode/ Parylene-C/ AuNPs/ Parylene-C/ ITO PET	Abrupt increase in current 2.6 and 10.4 V (Voltage range: 0 to +15 V)	-	• Lower voltage region: thermionic emission, Poole Frenkel–Schottky emission; • Medium voltage region: trapped charge limited current; • Higher voltage region: space charge limited current	[85]
Au electrode/ Pentacene/ PMSSQ/ nanocomposite with AuNPs/ PMSSQ/ ITO PET	V_{th}: +5.1 V; (Voltage range: 0 to +15 V)	V_{FB}: 9 V (Sweeping voltage range: 0–15 V)	• Lower voltage region: thermionic emission, Poole Frenkel–Schottky emission; • Medium voltage region: trapped charge limited current; • Higher voltage region:	[25]

			space charge limited current	
Al electrode/ PMSSQ/ AuNPs nanocomposite/ PMSSQ/ p-Si	V_{th}: 20 V	V_{FB}: 12 V	• Lower voltage region: thermionic emission; • Medium voltage region: Fowler–Nordheim; • Higher voltage region: space charge limited current	[87]
Al electrode/ PMSSQ/ AuNPs/ PMSSQ/ n-Si/ Al	V_{th}: 3.6 V with 6 order of current magnitude increment (sweeping voltage range:±10 V) I_{on}/I_{off} ratio: 10^4	V_{FB}: 3.6 V and 54 electrons trapped per AuNP	• Lower voltage region: thermionic emission; • Medium voltage region: trapped charge limited current; • Higher voltage region: space charge limited current	[52]
Au electrode/ PMSSQ/ AuNPs nanocomposite/ PMSSQ/ p-Si	Lower V_{th} is better choice due to lower programming voltage ~5.6 V (sweeping voltage range: ± 20 V) I_{on}/I_{off} ratio:10	-	• Lower voltage region: thermionic emission; • Medium voltage region: trapped charge limited current; • Higher voltage region:	[69]

			space charge limited current	
Au electrode/ PMSSQ/ AuNPs/ PMSSQ/ n-Si/ Al	V_{th} is 3.7 V	49	• Lower voltage region: thermionic emission, Poole Frenkel–Schottky emission; • Medium voltage region: trapped charge limited current; • Higher voltage region: space charge limited current	[58]
Au electrode/ PMSSQ/ AuNPs/ PMSSQ/ n-Si/ Al	V_{th} is 2.4	34	• Lower voltage region: thermionic emission, Poole Frenkel–Schottky emission; • Medium voltage region: trapped charge limited current; • Higher voltage region: space charge limited current	[57]
Au electrode/ PMSSQ/ AuNPs/ PMSSQ/ n-Si/ Al	V_{th} is 2.4	-	• Lower voltage region: thermionic emission, Poole	[56]

			Frenkel–Schottky emission; • Medium voltage region: trapped charge limited current; • Higher voltage region: space charge limited current	
Al electrode/ PMSSQ/ AuNPs/ PMSSQ/ n-Si/ Al	V_{th} is 3.6	54	• Lower voltage region: thermionic emission, Poole Frenkel–Schottky emission; • Medium voltage region: trapped charge limited current; • Higher voltage region: space charge limited current	[55]
Al electrode/ PVP/ AuNPs/ PVP/ Pentacene/Au	-	V_{FB}: 8.5 V at ±10 V sweep range; higher applied sweep voltage leads to a wider hysteresis and a memory window	-	[77]
Al electrode/PMSSQ/AuNPs nanocomposite/PMSSQ/p-Si	V_{th}: 13 V (Sweeping voltage range: 0-20 V)	-	• Lower voltage region: thermionic emission and	[88]

			Fowler–Nordheim; Medium voltage region: trapped charge limited current; • Higher voltage region: space charge limited current	
Au electrode/ Pentacene/ AuNPs/ APTES/ PVA/ P-type Si	-	V_{FB}: 5.4 V for (± 5 V); 8.6 V for (± 7 V)	-	[89]
Al/AuNPs + PVK/Al	I_{on}/I_{off} ratio up to 10^9	-	Charge transfer between PVK and AuNPs	[84]
Al/ pentacene/ AuNPs/ SiO_2/ p-Si	-	V_{FB}: 2.5 V (Sweeping voltage range: −9 V to 9 V)	-	[67]
Al electrode/ PS-b-P4VP/ AuNPs/ SiO2/ n-Si	-	V_{FB}: 0.34 V (pulse voltage= −6 V)	Schottky emission	[79]
Au electrode/ pentacene/ PS-b-P4VP/ SiO_2/ n-Si	-	Hysteresis window increases from 1.0, 2.6, and 6.8 V upon sweeping the gate voltage from 10, 20, and 30 V, respectively	-	[23]
Au electrode/ parylene/ AuNPs/ parylene/ Si	-	V_{FB}: 1.1 V	-	[90]
Pt electrode/ HfO_2/ AuNPs/ HfO_2/p-Si	-	V_{FB}: 1.9 V (sweeping voltage range ± 8 V)	-	[74]
Au electrode/ pentacene/	-	V_{FB}: 1.25–2.05 V	-	[91]

AuNPs/ APTES/ SiO_2/n-Si		sweeping voltage: 5–10 V		
Al_2O_3/AuNPs/SiO_2/p-Si	-	V_{FB}: 4.3 V (sweeping voltage range ±7 V)	-	[76]
Al/Au NPs+P3HT/Al	V_{th}: 3–4V; I_{on}/I_{off} ratio: 10^5	-	• Charge transfer between P3HT and AuNPs; • Off state: contact-limited Schottky emission; • On state: bulk-limited Poole–Frenkel emission	[92]
Al/AuNPs+8HQ+PS/Al	V_{th}: 2.8 V;	-	• Charge transfer between 8HQ and AuNPs; • On state: tunneling between 8HQ molecules	[5]
Au electrode/AuNPs/ Biotin-NHS/APTES/PVA/p-Si	-	ΔV_{FB} 1.2, 1.9, and 2.6 V upon voltage sweeping at 2,3, and 4 V	-	[78]

Conduction Mechanism

Analysis of the conduction mechanism in a nanoparticle-embedded polymer memory is important to facilitate technology development. Several mechanisms are normally applied to explain electron transport through dielectric films. These mechanisms include TE, PF emission, SE, SCLC, TCLC, and filamentary emission.

TE is the most common injection mechanism found in organic devices and occurs at a low voltage, as with direct tunneling. However, direct tunneling is suitable for samples with a thin insulating layer (~3 nm) [75]. TE transport mechanism is appropriate for insulator layers of ≥100 nm. TE involves heat-induced electrons from a semiconductor surface or hot metal emitted across a barrier. Figure 7.19 shows the energy band diagram of a TE electron over an insulator barrier.

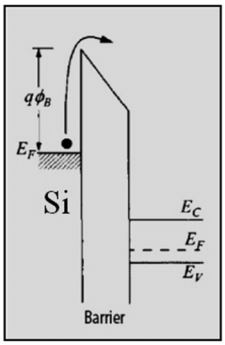

FIGURE 7.19
Energy band diagram of TE where the electron crosses over the insulator barrier

The TE conduction model is given as below:

$$I \propto T^2 \, exp\left[-\frac{q\emptyset_B}{kT} + q\sqrt{\frac{q^3 V}{4\pi\varepsilon_i}}\right], \tag{3}$$

where *T* is the absolute temperature, *q* is the electronic charge, *k* is the Boltzmann constant, *V* is the applied voltage, ε_i is the insulator permittivity, and $\emptyset_B$ is the barrier height. After deduction of TE conduction, the curve fitting of log (I/T^2) versus $V^{1/2}$becomes a straight line.
SE is a process in which carriers overcome the metal–insulator or the semiconductor–insulator interface barrier by TE through a field-assisted lowering of the barrier. SE is almost similar to TE. The energy diagram can be represented as in Figure 7.20, as the SE of the electron crosses over the barrier.

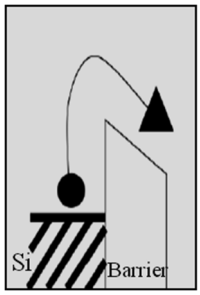

FIGURE 7.20
Energy band diagram of SE where the electron crosses over the insulator barrier

SE can be expressed by the Equation below [93]:

$$I \propto T^2 \, exp\left[-\frac{q}{kT}\left(\emptyset_B - \sqrt{\frac{qV}{4\pi d\varepsilon_i}}\right)\right], \tag{4}$$

where *T* is the absolute temperature, *q* is the electronic charge, *k* is the Boltzmann constant, *V* is

the applied voltage, ε_i is the insulator permittivity, and *d* is the insulator thickness. SE is also characterized by a linear relationship between the plot of log (I/T^2) versus $V^{1/2}$, as obtained in TE.
PF emission is a conduction mechanism that is highly similar to SE. It is sometimes called the internal SE. This conduction mechanism is dependent on insulating thin films. Thus, a large trap density should be thick enough to avoid quantum mechanical tunneling. Figure 7.21 shows the PF emission that the trapped electrons can pass through the conduction band due to the field-enhanced thermal excitation of external electric field or thermal activation. The energy barriers for PF conduction are within the molecules rather than at the molecule/contact interface [94, 95].

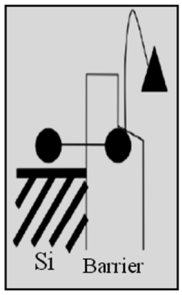

FIGURE 7.21
Energy band diagram showing the PF conduction mechanism

The *I–V* relation of a PF emission can be described as follows:

$$I \propto V exp\left[\frac{q}{kT}\left(\sqrt{\frac{qV}{\pi d\varepsilon_i}} - \emptyset_B\right)\right], \quad (5)$$

where *T* is the absolute temperature, *q* is the electronic charge, *k* is the Boltzmann constant, *V* is the applied voltage, ε_i is the insulator permittivity, $\emptyset_B$ is the barrier height, and *d* is the insulator thickness. A linear relation was observed between log (I/V) versus $V^{1/2}$ in the *I–V* characterization.
TCLC and SCLC can be predicted from double logarithmic *I–V* characteristics, with the current following the power law exponent in the form of $I \propto V^n$, where the value of *n* is obtained from the fitted slope. When *n* is more than 2 ($n > 2$), the model is defined as a TCLC mechanism. In TCLC conduction, an applied voltage injects free carriers into the device. The traps are gradually filled with increasing electric field, and the current increases faster until all traps are filled [96, 97].

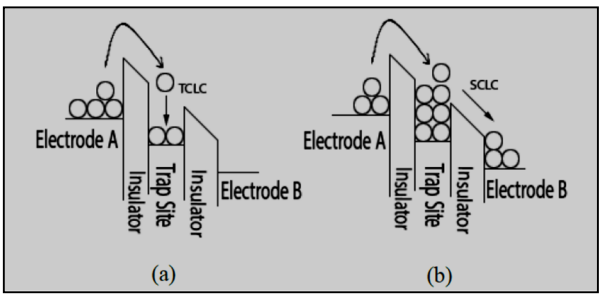

FIGURE 7.22
Energy band diagrams showing (a) TCLC and (b) SCLC conduction mechanisms [98]

According to previous work, the traps are filled up by the carriers through TCLC, after which the transition from TCLC to trap-free SCLC occurs [98]. Figure 7.22 shows the energy band diagrams of the transport mechanism of electrons for TCLC and SCLC.
SCLC is dominated by the presence of charge carrier traps. For instance, during the switching process in *I–V* characterization, excessive carriers are injected into the composites, and then the trap sites of nanoparticles are filled up with electrons, eventually causing SCLC. The Mott–Gurney model expresses the relationship between current and applied voltage by the following Equation [97, 99]:

$$I \propto \frac{9\varepsilon_i \mu V^2}{8d^3}, \tag{6}$$

where *V* is the applied voltage, ε_i is the insulator permittivity, μ is the carrier mobility, and *d* is the insulator thickness. The current is proportional to the square of the applied voltage, where $I \propto V^2$, and a plot of log I versus 2 log V is a straight line with a slope of $n \approx 2$ [100].

Band diagram of conduction mechanism

The band diagrams in Figure 7.23 illustrate the Au/PMSSQ2/nanocomposite/PMSSQ1/p-type Si memory device being programmed and erased. The electron emission flows from the Si into the AuNPs and then programs the device, as depicted in Figure 7.23(a). A similar negative pulse is applied at the Au electrode to attract the trapped electrons in the AuNPs back to the p-type Si and thus erase the device, as depicted in Figure 7.23(b). The emission of electrons from the Si substrate is preferable than that from Au electrodes. This result can be attributed to the low probability emission of electrons from Au electrodes when the work function of Au is 5.1 eV compared with the Fermi level of a lightly doped p-type Si of 4.91 eV.

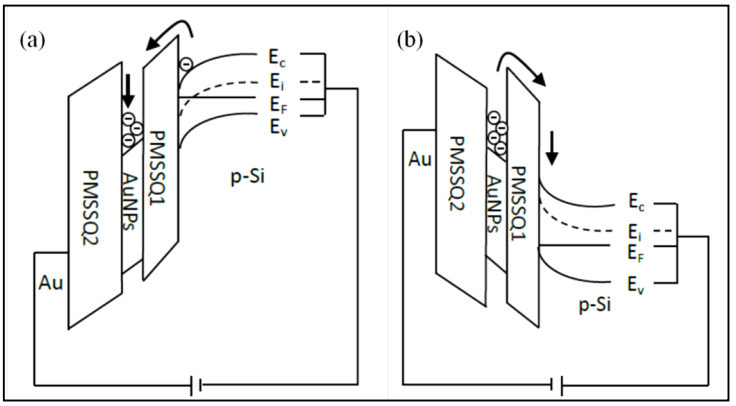

FIGURE 7.23
Band diagrams illustrate Au/PMSSQ 2/AuNP nanocomposite/PMSSQ 1/p-type Si memory device being (a) programmed and (b) erased [69]

The conduction mechanism of a device being programmed and erased in an organic memory device was studied by using band diagrams [25]. Figure 7.24 illustrates the band diagram of the Au/Pentacene/PMSSQ 2/AuNP nanocomposite/PMSSQ 1/ITO-coated PET memory device being programmed and erased as voltage was applied at the Au electrode. The device was programmed

when electrons were trapped in the AuNPs, and the device was erased with the void of trapped electrons in the AuNPs, as shown in Figure 7.24(a). To program the device, an arbitrary large positive voltage was applied at the Au electrode to inject electrons into the AuNPs from the ITO. In addition, a similar pulse with a negative value was applied at the Au electrode in an attempt to push the trapped electrons out from the AuNPs toward the ITO and thus erase the device, as shown in Figure 7.24(b).

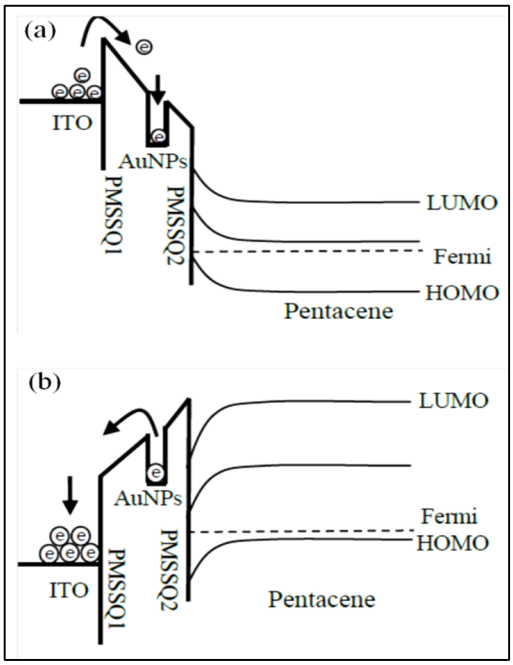

FIGURE 7.24
Band diagrams illustrated Au/Pentacene/PMSSQ 2/AuNP nanocomposite/PMSSQ 1/ITO coated PET being (a) programmed and (b) erased [25]

Future outlook

AuNP thin films have the potential to be used in hybrid NVM applications. The main challenge is the fabrication of AuNP thin films directly on the substrates where only a certain size of AuNPs and distribution can contribute to the enhancement of charge storage. The interaction of AuNPs with organic dielectric materials is also important; favorable adhesion is necessary to obtain favorable properties. Moreover, fabrication temperature must be low enough to compensate for the low glass transition temperature of the organic polymer. For hybrid memory device development, further research should focus on fabricating or searching for devices that can store more charges and require a low power to turn “ON” the voltage. The high demand in flexible NVMs and transparent memories is also of interest for future development.

References

1. Heremans, P., et al., *Polymer and organic nonvolatile memory devices†.* Chemistry of Materials, 2010. **23**(3): p. 341-358.
2. Meena, J.S., et al., *Overview of emerging nonvolatile memory technologies.* Nanoscale Research Letters, 2014. **9**(1): p. 1-33.
3. Burr, G.W., et al., *Phase change memory technology.* Journal of Vacuum Science & Technology B, 2010. **28**(2): p. 223-262.
4. Wang, H., et al., *Nonvolatile memory devices based on organic field-effect transistors.* Chinese Science Bulletin, 2011. **56**(13): p. 1325-1332.
5. Ouyang, J., et al., *Organic Memory Device Fabricated Through Solution Processing.* Proceedings of the IEEE, 2005. **93**(7): p. 1287-1296.
6. Chen, W.-R., et al., *Formation and Nonvolatile Memory Application of Ge Nanocrystals by Using Internal Competition Reaction of and Layers.* Nanotechnology, IEEE Transactions on, 2009. **8**(2): p. 185-189.
7. Tiwari, S., et al., *A silicon nanocrystals based memory.* Applied Physics Letters, 1996. **68**(10): p. 1377-1379.
8. Lee, C., A. Gorur-Seetharam, and E.C. Kan. *Operational and reliability comparison of discrete-storage nonvolatile memories: Advantages of single-and double-layer metal nanocrystals*. in *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*. 2003: IEEE.
9. Zhao, D., Y. Zhu, and J. Liu, *Charge storage in a metal–oxide–semiconductor capacitor containing cobalt nanocrystals.* Solid-state electronics, 2006. **50**(2): p. 268-271.
10. Lee, C., T.-H. Hou, and E.C.-C. Kan, *Nonvolatile memory with a metal nanocrystal/nitride heterogeneous floating-gate.* Electron Devices, IEEE Transactions on, 2005. **52**(12): p. 2697-2702.
11. Park, B., et al., *Electrical Characteristics of Floating-Gate Memory Devices with Titanium Nanoparticles Embedded in Gate Oxides.* Journal of nanoscience and nanotechnology, 2009. **9**(3): p. 1904-1908.
12. Lee, J.J. and D.-L. Kwong, *Metal nanocrystal memory with high-κ tunneling barrier for improved data retention.* Electron Devices, IEEE Transactions on, 2005. **52**(4): p. 507-511.
13. Chang, T.-C., et al., *Developments in nanocrystal memory.* Materials today, 2011. **14**(12): p. 608-615.
14. Kim, Y.-H., et al., *Organic Memory Capacitor Device Fabricated with Ag Nanoparticles.* Journal of nanoscience and nanotechnology, 2011. **11**(7): p. 6044-6048.
15. Choi, H., et al., *Memory characteristics of a self-assembled monolayer of Pt nanoparticles as a charge trapping layer.* Nanotechnology, 2008. **19**(30): p. 305704.
16. Lee, J.-S., *Recent progress in gold nanoparticle-based non-volatile memory devices.* Gold Bulletin, 2010. **43**(3): p. 189-199.
17. Daniel, M.-C. and D. Astruc, *Gold nanoparticles: assembly, supramolecular chemistry, quantum-size-related properties, and applications toward biology, catalysis, and nanotechnology.* Chemical reviews, 2004. **104**(1): p. 293-346.
18. Boisselier, E. and D. Astruc, *Gold nanoparticles in nanomedicine: preparations, imaging, diagnostics, therapies and toxicity.* Chemical Society Reviews, 2009. **38**(6): p. 1759-1782.
19. Huang, X. and M.A. El-Sayed, *Gold nanoparticles: optical properties and implementations in cancer diagnosis and photothermal therapy.* Journal of Advanced Research, 2010. **1**(1): p. 13-28.

20. Lee, J.-H., et al., *Production of aqueous spherical gold nanoparticles using conventional ultrasonic bath.* Nanoscale Research Letters, 2012. **7**(1): p. 1-7.
21. Kim, T.W., et al., *Electrical memory devices based on inorganic/organic nanocomposites.* NPG Asia Mater, 2012. **4**: p. e18.
22. Park, I., et al., *Nanoscale patterning and electronics on flexible substrate by direct nanoimprinting of metallic nanoparticles.* Advanced Materials, 2008. **20**(3): p. 489-496.
23. Leong, W.L., et al., *Non-Volatile Organic Memory Applications Enabled by In Situ Synthesis of Gold Nanoparticles in a Self-Assembled Block Copolymer.* Advanced Materials, 2008. **20**(12): p. 2325-2331.
24. Lee, J.-K., et al., *Synthetic control of molecular weight and microstructure of processible poly (methylsilsesquioxane) s for low-dielectric thin film applications.* Polymer, 2001. **42**(21): p. 9085-9089.
25. Ooi, P.C., et al., *An optically transparent and flexible memory with embedded gold nanoparticles in a polymethylsilsesquioxane dielectric.* Thin Solid Films, 2013. **544**(0): p. 597-601.
26. Yang, Y., et al., *Electrical Switching and Bistability in Organic/Polymeric Thin Films and Memory Devices.* Advanced Functional Materials, 2006. **16**(8): p. 1001-1014.
27. Ma, L., et al., *Nonvolatile electrical bistability of organic/metal-nanocluster/organic system.* Applied Physics Letters, 2003. **82**(9): p. 1419-1421.
28. Adschiri, T. and K. Byrappa, *Supercritical hydrothermal synthesis of organic-inorganic hybrid nanoparticles*, in *Nanohybridization of Organic-Inorganic Materials*. 2009, Springer. p. 247-280.
29. Schmid, G., *Large clusters and colloids. Metals in the embryonic state.* Chemical reviews, 1992. **92**(8): p. 1709-1727.
30. Brust, M. and C.J. Kiely, *Some recent advances in nanostructure preparation from gold and silver particles: a short topical review.* Colloids and Surfaces A: Physicochemical and Engineering Aspects, 2002. **202**(2): p. 175-186.
31. Talapin, D.V., et al., *Prospects of colloidal nanocrystals for electronic and optoelectronic applications.* Chemical reviews, 2009. **110**(1): p. 389-458.
32. Su, S., et al., *Design and applications of gold nanoparticle conjugates by exploiting biomolecule-gold nanoparticle interactions.* Nanoscale, 2013. **5**(7): p. 2589-2599.
33. Eustis, S. and M.A. El-Sayed, *Why gold nanoparticles are more precious than pretty gold: noble metal surface plasmon resonance and its enhancement of the radiative and nonradiative properties of nanocrystals of different shapes.* Chemical Society Reviews, 2006. **35**(3): p. 209-217.
34. Jain, P.K., et al., *Noble metals on the nanoscale: optical and photothermal properties and some applications in imaging, sensing, biology, and medicine.* Accounts of Chemical Research, 2008. **41**(12): p. 1578-1586.
35. Personick, M.L., et al., *Synthesis and isolation of {110}-faceted gold bipyramids and rhombic dodecahedra.* Journal of the American Chemical Society, 2011. **133**(16): p. 6170-6173.
36. Mody, V.V., et al., *Introduction to metallic nanoparticles.* Journal of Pharmacy and Bioallied Sciences, 2010. **2**(4): p. 282.
37. Leong, W.L., et al., *Towards printable organic thin film transistor based flash memory devices.* Journal of Materials Chemistry, 2011. **21**(14): p. 5203-5214.
38. Liu, F.-K., et al., *Rapid fabrication of high quality self-assembled nanometer gold particles by spin coating method.* Microelectronic Engineering, 2003. **67–68**(0): p. 702-709.

39. Das, A., S. Das, and A.K. Raychaudhuri, *Growth of two-dimensional arrays of uncapped gold nanoparticles on silicon substrates.* Bulletin of Materials Science, 2008. **31**(3): p. 277-282.
40. Hurst, K.M., et al., *Self-assembled monolayer-immobilized gold nanoparticles as durable, anti-stiction coatings for MEMS.* Microelectromechanical Systems, Journal of, 2011. **20**(2): p. 424-435.
41. Leu, C.-C., S.-T. Chen, and F.-K. Liu, *Spin-Coating-Derived Gold-Nanoparticle Memory.* Journal of the American Ceramic Society, 2010. **93**(10): p. 3142-3147.
42. Huang, K.-W., et al., *Improved performance of aminopropylsilatrane over aminopropyltriethoxysilane as a linker for nanoparticle-based plasmon resonance sensors.* Sensors and Actuators B: Chemical, 2012. **163**(1): p. 207-215.
43. Shipway, A.N., E. Katz, and I. Willner, *Nanoparticle arrays on surfaces for electronic, optical, and sensor applications.* ChemPhysChem, 2000. **1**(1): p. 18-52.
44. Gupta, R.K., et al., *Covalent assembly of gold nanoparticles for nonvolatile memory applications.* ACS applied materials & interfaces, 2011. **3**(12): p. 4619-4625.
45. Akutagawa, T., T. Nakamura, and J. Becher, *Molecular assembly of nanowires*. 2004, Dekker Encyclopedia of Nanoscience and Nanotechnology. p. 2019-2024.
46. Paul, S., et al., *Langmuir-Blodgett film deposition of metallic nanoparticles and their application to electronic memory structures.* Nano Lett, 2003. **3**: p. 533.
47. Chitu, L., et al., *Modified Langmuir-Blodgett deposition of nanoparticles - measurement of 2D to 3D ordered arrays*, in *Measurement Science Review*. 2010. p. 162.
48. Huang, J., et al., *Spontaneous formation of nanoparticle stripe patterns through dewetting.* Nat Mater, 2005. **4**(12): p. 896-900.
49. Liu, Z., et al., *Metal nanocrystal memories. I. Device design and fabrication.* Electron Devices, IEEE Transactions on, 2002. **49**(9): p. 1606-1613.
50. Ratautas, K., et al., *Transformation of a Thin Gold Film to Nanoparticles after Nanosecond–Laser Irradiation.* JOURNAL OF LASER MICRO NANOENGINEERING, 2012. **7**(3): p. 355-361.
51. Gaspar, D., et al., *Influence of the layer thickness in plasmonic gold nanoparticles produced by thermal evaporation.* Scientific reports, 2013. **3**.
52. Goh, L., et al., *Direct formation of gold nanoparticles on substrates using a novel ZnO sacrificial templated-growth hydrothermal approach and their properties in organic memory device.* Nanoscale Research Letters, 2012. **7**(1): p. 563.
53. Rue, A.E. and M.M. Collinson, *Size and shape control of gold nanodeposits in an array of silica nanowells on a gold electrode.* International Journal of Electrochemistry, 2012. **2012**.
54. Gupta, R., et al., *Enhancing charge-storage capacity of non-volatile memory devices using template-directed assembly of gold nanoparticles.* Nanoscale, 2012. **4**: p. 2296.
55. Ng, S.A., et al. *Effect of Zinc Nitrate Concentration on Formation of AuNPs by Sacrificial Templated Growth Hydrothermal Approach and its Properties in Organic Memory Device*. in *Advanced Materials Research*. 2014: Trans Tech Publ.
56. Ng, S.A., et al. *The Effect of Hydrothermal Reaction Time on Formation of AuNPs by Sacrificial Templated Growth Hydrothermal Approach*. in *Advanced Materials Research*. 2014: Trans Tech Publ.
57. Ng, S.A., et al., *Growth of gold nanoparticles using aluminum template via low-temperature hydrothermal method for memory applications.* Journal of Materials Science: Materials in Electronics, 2015: p. 1-11.
58. Ng, S.A., et al., *Direct formation of AuNPs thin film using thermal evaporated zinc as sacrificial template in hydrothermal method.* Journal of Materials Science: Materials in Electronics, 2014. **25**(5): p. 2227-2236.

59. Li, W., et al., *Superlattice structure of gold nanoparticles film deposited by Langmuir-Blodgett technique.* Molecular Crystals and Liquid Crystals, 1999. **337**(1): p. 185-188.
60. Sajanlal, P.R., et al., *Anisotropic nanomaterials: structure, growth, assembly, and functions.* Nano reviews, 2011. **2**: p. 5883_1-5883_62.
61. Sanchez-Mendieta, V. and A.R. Vilchis-Nestor, *Green synthesis of noble metal (Au, Ag, Pt) nanoparticles, assisted by plant-extracts*. 2012: INTECH Open Access Publisher.
62. Premkumar, T., K. Lee, and K.E. Geckeler, *Shape-tailoring and catalytic function of anisotropic gold nanostructures.* Nanoscale Research Letters, 2011. **6**(1): p. 1-12.
63. Chang, S.L., et al., *Stability of porous platinum nanoparticles: Combined in situ TEM and theoretical study.* The Journal of Physical Chemistry Letters, 2012. **3**(9): p. 1106-1110.
64. Harwell, K., *World Gold Council (www. gold. org).* Journal of Business & Finance Librarianship, 2009. **14**(2): p. 188-194.
65. Lide, D.R., *CRC handbook of chemistry and physics*. 2004: CRC press. 12-144.
66. Jian, L., et al., *Nonvolatile memory devices based on gold nanoparticle and poly (N-Vinylcarbazole) composite.* Chinese Physics Letters, 2007. **24**(11): p. 3280.
67. Mabrook, M.F., et al., *Memory effects in hybrid silicon-metallic nanoparticle-organic thin film structures.* Organic Electronics, 2008. **9**(5): p. 816-820.
68. Zhen, L., et al., *Organic thin-film transistor memory with gold nanocrystals embedded in polyimide gate dielectric.* Journal of Physics D: Applied Physics, 2008. **41**(13): p. 135111.
69. Ooi, P.C., et al., *Effects of metal electrodes and dielectric thickness on non-volatile memory with embedded gold nanoparticles in polymethylsilsesquioxane.* Microelectronic Engineering, 2012. **98**(0): p. 74-79.
70. Zhou, Y., et al., *Low voltage flexible nonvolatile memory with gold nanoparticles embedded in poly (methyl methacrylate).* Nanotechnology, 2012. **23**(34): p. 344014.
71. Bozano, L., et al., *Mechanism for bistability in organic memory elements.* Applied Physics Letters, 2004. **84**(4): p. 607-609.
72. Ma, L., J. Liu, and Y. Yang, *Organic electrical bistable devices and rewritable memory cells.* Applied Physics Letters, 2002. **80**(16): p. 2997-2999.
73. Lee, W., et al., *An organic thin film transistor based non-volatile memory with zinc oxide nanoparticles.* Thin Solid Films, 2011. **519**(15): p. 5208-5211.
74. Yang, J., et al., *Electrostatic force microscopy measurements of charge trapping behavior of Au nanoparticles embedded in metal–insulator–semiconductor structure.* Ultramicroscopy, 2008. **108**(10): p. 1215-1219.
75. Lu, T., et al., *Multilevel charge storage in silicon nanocrystal multilayers.* Applied Physics Letters, 2005. **87**(20): p. 202110.
76. Park, B., et al., *Capacitance characteristics of MOS capacitors embedded with colloidally synthesized gold nanoparticles.* Semiconductor science and technology, 2006. **21**(7): p. 975.
77. Sleiman, A., et al. *Gold nanoparticles as a floating gate in Pentacene/PVP based MIS memory devices*. in *Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on*. 2012: IEEE.
78. Jung, S.M., et al., *Charging effect in Au nanoparticle memory device with biomolecule binding mechanism.* Journal of nanoscience and nanotechnology, 2011. **11**(7): p. 5698-5701.
79. Leong, W., et al., *Charging dynamics of discrete gold nanoparticle arrays self-assembled within a poly (styrene-b-4-vinylpyridine) diblock copolymer template.* Applied Physics Letters, 2008. **93**(22): p. 222908-222908-3.
80. Miura, A., et al., *Floating nanodot gate memory fabrication with biomineralized nanodot as charge storage node.* Journal of Applied Physics, 2008. **103**(7): p. -.

81. Zhou, Y., et al., *Nonvolatile multilevel data storage memory device from controlled ambipolar charge trapping mechanism.* Scientific reports, 2013. **3**.
82. Prime, D., S. Paul, and P. Josephs-Franks, *Gold nanoparticle charge trapping and relation to organic polymer memory devices.* Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences, 2009. **367**(1905): p. 4215-4225.
83. Prime, D. and S. Paul, *Overview of organic memory devices.* Phil Trans R Soc A, 2009. **367**: p. 4141.
84. Lai, P.Y. and J.-S. Chen, *Electrical bistability and charge transport behavior in Au nanoparticle/poly (N-vinylcarbazole) hybrid memory devices.* Applied Physics Letters, 2008. **93**(15): p. 153305-153305-3.
85. Aw, K.C., et al., *A transparent and flexible organic bistable memory device using parylene with embedded gold nanoparticles.* Journal of Materials Science: Materials in Electronics, 2013. **24**(8): p. 3116-3125.
86. Lin, H.-T., Z. Pei, and Y.-J. Chan, *Carrier transport mechanism in a nanoparticle-incorporated organic bistable memory device.* Electron Device Letters, IEEE, 2007. **28**(7): p. 569-571.
87. Ahmad, Z., et al., *Programmable nonvolatile memory based on gold nanoparticles in poly-methyl-silsesquioxane sol–gel.* Microelectronic Engineering, 2012. **99**(0): p. 62-66.
88. Ahmad, Z., et al., *Electrical characteristics of poly (methylsilsesquioxane) thin films for non-volatile memory.* Solid State Communications, 2011. **151**(4): p. 297-300.
89. Kim, A., et al., *All solution-processed, fully transparent resistive memory devices.* ACS applied materials & interfaces, 2011. **3**(11): p. 4525-4530.
90. Park, B., et al., *Electrical characteristics of gold nanoparticle-embedded MIS capacitors with parylene gate dielectric.* Org Electron, 2008. **9**: p. 878.
91. Leong, W., et al., *Charging phenomena in pentacene-gold nanoparticle memory device.* Applied Physics Letters, 2007. **90**(4): p. 042906.
92. Prakash, A., et al., *Polymer memory device based on conjugated polymer and gold nanoparticles.* J Appl Phys, 2006. **100**: p. 054309.
93. Rahman, M., et al., *Current transport mechanism in high-κ cerium oxide gate dielectrics grown on Germanium substrates.* Electrochemical and Solid-State Letters, 2009. **12**(5): p. H165-H168.
94. Verma, A., P. Khare, and R.K. Srivastava, *Electrode effect on electrical conduction in thin film of polyvinyl pyrrolidone.* Indian Journal of Pure & Applied Physics, 2009. **47**: p. 737-744.
95. Kwon, H.-M., et al., *Conduction Mechanism and Reliability Characteristics of a Metal–Insulator–Metal Capacitor with Single ZrO2 Layer.* Japanese Journal of Applied Physics, 2011. **50**(4S): p. 04DD02.
96. Khan, M., et al., *Electron injection and transport mechanism in organic devices based on electron transport materials.* Journal of Physics D: Applied Physics, 2008. **41**(22): p. 225105.
97. Brütting, W., S. Berleb, and A. Mückl, *Space-charge limited conduction with a field and temperature dependent mobility in Alq light-emitting devices.* Synthetic metals, 2001. **122**(1): p. 99-104.
98. Yamamoto, H., et al., *Extremely-high-density carrier injection and transport over 12000A/cm2 into organic thin films.* Applied Physics Letters, 2005. **86**(8): p. 083502.
99. Sze, S.M. and K.K. Ng, *Physics of semiconductor devices*. 3rd ed. 2007, Hoboken: John Wiley & Sons.
100. Cho, B., et al., *Organic resistive memory devices: performance enhancement, integration, and advanced architectures.* Advanced Functional Materials, 2011. **21**(15): p. 2806-2829.

List of symbols

eV	Electron volt
GPa	GigaPascal
nm	Nanometer
mTorr	Milltorr
W	Watt
SCCM	Standard cubic centimeters per minute
ΔG	Gibbs free energy
V_{TH}	Threshold voltage
I_{ON}/I_{OFF}	On-off current ratio
ε_i	Insulator permittivity
q	Electronic charge
k	Boltzmann constant
V	Voltage
$Ø_B$	Barrier height
d	Insulator thickness
μ	Carrier mobility
$\propto$	Proportional to
$\approx$	Approximately
V_{FB}	Flat band voltage

List of acronyms

NVM	non-volatile memory
FG	Floating gate
Si	Silicon
Ge	Germanium
Al	Aluminium
Au	Gold
Ag	Silver
Pt	Platinum
PS-b-P4VP	Polystyrene-block-poly(4-vinylpyridine)
PMSSQ	Polymethylsiloxane
AuNPs	Gold nanoparticles
SPR	Surface plasmon resonance
LB	Langmuir-Blodgett
APhTS	p-aminophenyl trimethoxysilane
MPTS	3-mercaptopropyl trimethoxysilane
APS	aminopropylsilatrane
APTES	3-aminopropyltriethoxysilane
MUD	11-mercapto-1-undecanol
TEM	Transmission electron microscope
PS	Polystyrene
$HAuCl_4$	Gold(III)chloride trihydrate

NH_2OH	Hydroxylamine
PS-b-PVP	Polystyrene-block-poly(2-vinylpyridine)
ZnO	Zinc oxide
$Zn(NO_3)_2.4H2O$	Zinc nitrate tetrahydrate
$C_6H_{12}N_4$	hexamethylenetetramine
C-V	Capacitance-voltage
I-V	Current-voltage
Al_2O_3	Aluminum Oxide
SCLC	Trap-limited space charge limited current
TCLC	Trapped charge limited current
TE	Thermionic emission
PF	Poole-Frenkel
ITO	Indium-titanium-oxide
RIE	Reactive ion etching
MIS	Metal-Insulator-Semiconductor